REMARKS

With the above amendments, claims 1-4, 6-15, and 17-18 remain in the application. Claims 5 and 16 are hereby canceled without prejudice. Claims 1, 4, 8, 12, 14 and 18 are hereby amended. No new matter is being added.

Objections to the Specification

In paragraph 5 of the latest office action, the title of the invention is objected to. Applicants hereby amend the title per the suggestion of the Examiner. As such, applicants respectfully submit that this objection is now overcome.

In paragraph 6 of the latest office action, the disclosure is objected to due to an embedded hyperlink. Applicants hereby amend page 7 of the specification so as to remove that hyperlink. As such, applicants respectfully submit that this objection is now overcome.

In paragraph 7 of the latest office action, the disclosure is objected to as not providing antecedent basis for "logical analysis" as used in original claim 4. Applicants hereby amend claim 4 so as to remove the "logical analysis" language. As such, applicants respectfully submit that this objection is now overcome.

Objections to the Claims

In paragraph 9 of the latest office action, claim 1 is objected to for the phrase "an fault storage unit." In accordance with the Examiner's recommendation, claim 1 is now amended to read --a fault storage unit--. As such, applicants respectfully submit that this objection is now overcome.

In paragraphs 10 and 11 of the latest office action, claims 2 and 7 objected to for the phrase "the particular memory module" which refers to "that particular memory module" in claim 1. Claim 1 is now amended to replace "that particular memory module" with --the particular memory module--. As such, applicants respectfully submit that this objection is now overcome.

In paragraph 12 of the latest office action, claim 15 is objected to for insufficient antecedent basis for "the entries." Claim 15 depends from claim 12. Claim 12 is now amended so as to recite "entries" as antecedent basis for "the entries" in claim 15. As such, applicants respectfully submit that this objection is now overcome.

Claim Rejections under 35 U.S.C. § 112

In paragraph 14 of the latest office action, claim 4 is rejected due to the claim language "logical analysis." Claim 4 is now amended and no longer recites that claim language. As such, applicants respectfully submit that this rejection is now moot.

In paragraph 16 of the latest office action, claim 12 is rejected due to the phrase "configured to connect to." Claim 12 is now amended so as to replace that phrase with --connects to--. As such, applicants respectfully submit that this rejection is now overcome.

Claim Rejections under 35 U.S.C. § 102 or § 103

The pending claims stand rejected under 35 U.S.C. § 102 or 103 as anticipated by or unpatentable over various cited art. These rejections are respectfully traversed for the claims as now amended.

Claim 1 as amended now recites as follows.

1. A method for persistently tracking volatile memory faults, the method comprising:
detecting a memory error relating to at least one dynamic random access memory (DRAM) unit on a particular memory module; and
writing an entry pertaining to the memory error in non-volatile memory of a fault storage unit on the particular memory module,
wherein **the entry comprises** a DRAM unit identifier, a start bit of the memory error, an end bit of the memory error, and **tag bits indicating time of last failure and number of occurrences of failure**.

(Emphasis added.)

As shown above, claim 1 now recites "**writing an entry pertaining to the memory error in non-volatile memory of a fault storage unit on the particular memory module,**" and that "**the entry comprises a DRAM unit identifier, a start bit of the memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.**" (Emphasis added.)

The above-recited limitations find support on page 10, lines 13-24 of the original specification, which recites as follows.

> In one implementation, the fields include a DRAM number **602**, a start bit of the memory error **604**, and an end bit of the memory error **606**. **The DRAM number 602 indicates a specific DRAM chip on the memory module in which the error is located. The bit range in the DRAM which includes the faulty memory bits are indicated by the start 604 and end 606 bits**. If the group of bits related to a memory error are not contiguous, then more than one entry would be used to store the memory error information in the fault storage unit.

> Other implementations of the memory error table may also be used in accordance with other embodiments of the invention. For example, **additional fields may be included, such as, for example, a field indicating the last time at which the memory error was detected and the number of times the bit range has failed.**

(Emphasis added.)

Jeddeloh '314 neither teaches nor suggests the above-recited limitations to the entry written into the non-volatile memory of the memory module. In particular, while Jeddeloh '314 discloses writing an "error map," Jedelloh '314 neither teaches nor suggests **writing entries into the non-volatile memory of the memory module which identify a failed bit range and which include tag bits indicating time of last failure and number of occurrences of failure.**

Moreover, the other cited art (Jeddeloh '798, Abel et al., Raynham '647, Bowden et al., Galanti, and Cepulis et al.) also do not teach or suggest writing entries into the non-volatile memory of the memory module which identify a failed bit range and which include tag bits indicating time of last failure and number of occurrences of failure.

Hence, applicants respectfully submit that claim 1, as amended, is now patentably distinguished over the cited art.

Claims 2- 4 and 6-7 depend from claim 1. As such, claims 2-4 and 6-7 are patentable over the cited art for at least the same reasons discussed above in relation to claim 1.

Regarding independent claim 8, claim 8 as amended now recites as follows.

8. **A memory module** that persistently tracks volatile memory faults, the memory module **comprising**:
a plurality of dynamic random access memories (DRAMs); and
a fault storage unit including non-volatile memory configured to store entries pertaining to faults in the plurality of DRAMs on that memory module,
wherein **each said entry comprises a DRAM unit identifier, a start bit of a memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.**

(Emphasis added.)

As shown above, claim 8 as amended now requires **entries stored in the non-volatile memory of the memory module, wherein each entry identifies a failed bit range and that includes tag bits indicating time of last failure and number of occurrences of failure.**

Jeddeloh '314 neither teaches nor suggests the above-recited limitations to the entry written into the non-volatile memory of the memory module. In particular, while Jeddeloh '314 discloses writing an "error map," Jedelloh '314 neither teaches nor suggests entries stored in the non-volatile memory of the memory module, wherein each entry identifies a failed bit range and that includes tag bits indicating time of last failure and number of occurrences of failure.

Moreover, the other cited art (Jeddeloh '798, Abel et al., Raynham '647, Bowden et al., Galanti, and Cepulis et al.) also do not teach or suggest entries stored in the non-volatile memory of the memory module, wherein each entry identifies a failed bit range and that includes tag bits indicating time of last failure and number of occurrences of failure.

Hence, applicants respectfully submit that claim 8, as amended, is now patentably distinguished over the cited art.

Claims 9-11 depend from claim 8. As such, claims 9-11 are patentable over the cited art for at least the same reasons discussed above in relation to claim 8.

Regarding independent claim 12, claim 12 as amended now recites as follows.

> 12. A circuit board of a system, the circuit board comprising:
> a plurality of connectors, each connector connects to a memory module which includes multiple volatile memory units and a non-volatile fault storage unit;
> a memory controller configured to read and write data into the volatile memory units of memory modules;
> a memory error interface configured to provide read and write access to the non-volatile fault storage units of the memory modules; and
> **error handling code including instructions to write entries relating to detected memory errors into the non-volatile fault storage unit and to read said entries from the non-volatile fault storage unit,**
> wherein **each said entry comprises a memory unit identifier, a start bit of a memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.**

(Emphasis added.)

As shown above, claim 12 as amended now requires **error handling code which writes/reads entries into/from the non-volatile fault storage unit, wherein**

each entry identifies a failed bit range and that includes tag bits indicating time of last failure and number of occurrences of failure.

Jeddeloh '314 neither teaches nor suggests the above-recited limitations to the error handling code. In particular, while Jeddeloh '314 discloses writing an "error map," Jedelloh '314 neither teaches nor suggests error handling code which writes/reads entries into/from the non-volatile fault storage unit, wherein each entry identifies a failed bit range and that includes tag bits indicating time of last failure and number of occurrences of failure.

Moreover, the other cited art (Jeddeloh '798, Abel et al., Raynham '647, Bowden et al., Galanti, and Cepulis et al.) also do not teach or suggest entries stored in the non-volatile fault storage unit, wherein each entry identifies a failed bit range and that includes tag bits indicating time of last failure and number of occurrences of failure.

Hence, applicants respectfully submit that claim 12, as amended, is now patentably distinguished over the cited art.

Claims 13-15 and 17 depend from claim 12. As such, claims 13-15 and 17 are patentable over the cited art for at least the same reasons discussed above in relation to claim 12.

Regarding claim 18, claim 18 as amended now recites as follows.

18. A memory system comprising:
means for reading data from and writing data to volatile memory units on a plurality of memory modules; and
means for reading error entries from and writing error entries to a non-volatile fault storage unit on each memory module,

wherein **an error entry comprises a DRAM unit identifier, a start bit of a memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.**

(Emphasis added.)

As shown above, claim 18 as amended now requires **means for writing entries into the non-volatile memory of the memory module which identify a failed bit range and which include tag bits indicating time of last failure and number of occurrences of failure.**

Jeddeloh '314 neither teaches nor suggests the above-recited limitations. In particular, while Jeddeloh '314 discloses writing an "error map," Jedelloh '314 neither teaches nor suggests means for writing entries into the non-volatile memory of the memory module which identify a failed bit range and which include tag bits indicating time of last failure and number of occurrences of failure.

Moreover, the other cited art (Jeddeloh '798, Abel et al., Raynham '647, Bowden et al., Galanti, and Cepulis et al.) also do not teach or suggest means for writing entries into the non-volatile memory of the memory module which identify a failed bit range and which include tag bits indicating time of last failure and number of occurrences of failure.

Hence, applicants respectfully submit that claim 18, as amended, is now patentably distinguished over the cited art.

Conclusion

For at least the above reasons, it is respectfully submitted that claims 1-4, 6-15, and 17-18 are now patentably distinguished over the cited art. The Examiner is invited to telephone the undersigned at (408) 436-2111 for any questions.

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 08-2025.

Respectfully submitted,
Ken Gary Pomaranski, et al.

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James K. Okamoto, Reg. No. 40,110
Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164
Tel.: (408)436-2110
Fax.: (408)436-2114

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